**Nixie Tube Driver Test Jig – Principle of Operation**

**Requirements**

The nixie tube driver test jig (henceforth known as NTDTJ) is a bed of nails platform on which a single nixie tube driver (NTD) can be placed, which will automate the process of testing the functionality of the NTD. It should be able to test every digit in every segment of the NTD for correct functionality, alongside the high voltage (HV) connection to each segment. It should also light the RGB backlight LEDs for a human visual inspection.

Any errors encountered in the test should be reported back to the operator via a serial terminal, the error reporting should be comprehensive, explaining in detail where an error was found, and what kind of error it was.

**Nixie Tube Driver Principle of Operation**

To understand the principle of operations of the NTDTJ it is required that the principle of operations of the NTD itself is understood.

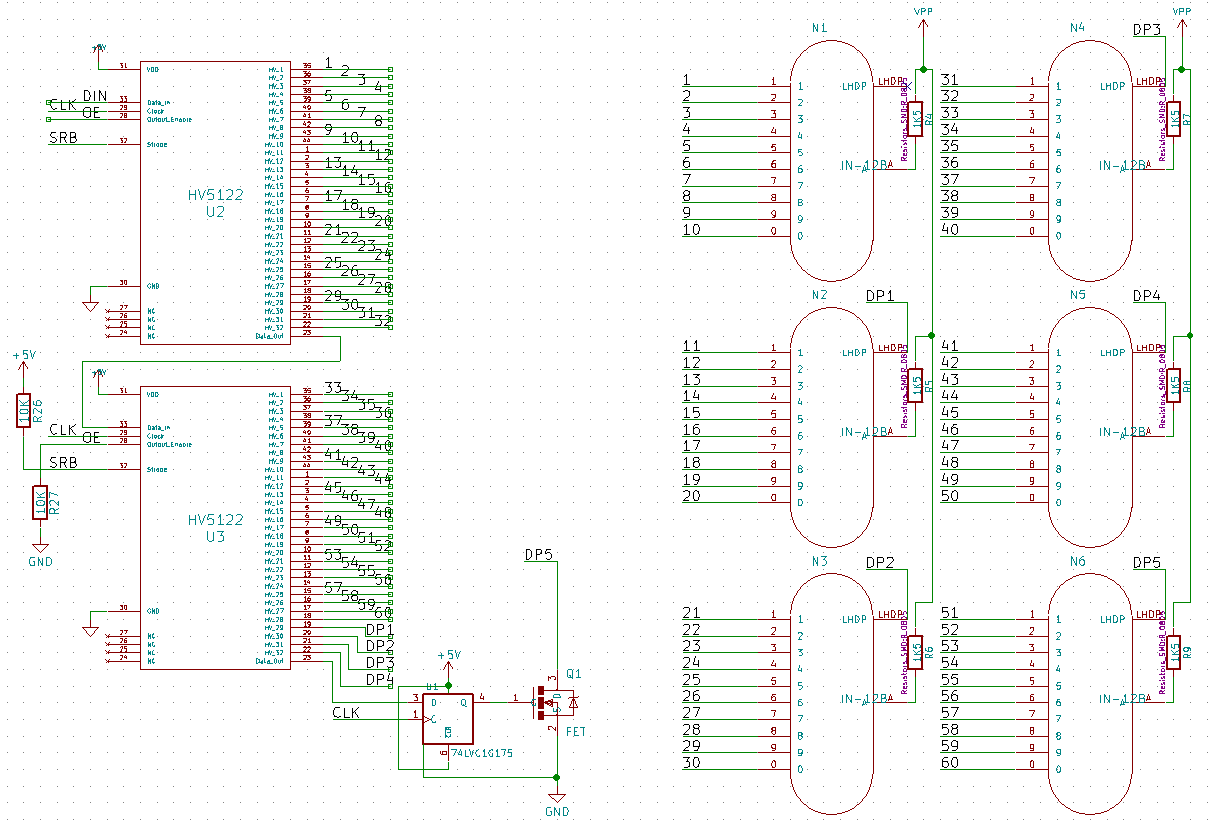
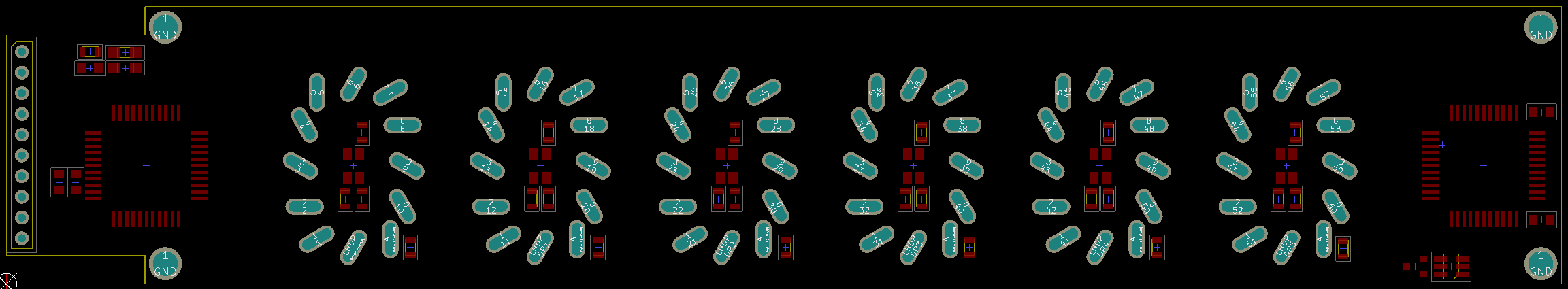
The NTD is essentially a 65-bit open drain shift register. It consists of 2 HV5122 High Voltage shift registers in series, followed by a single D-type flip flop with its output to an open drain MOSFET configuration. The schematic is given below.

Figure - NTD Schematic (incomplete)

The segments and digits on the NTD are arranged in the following manner:



Segment 0

Segment 1

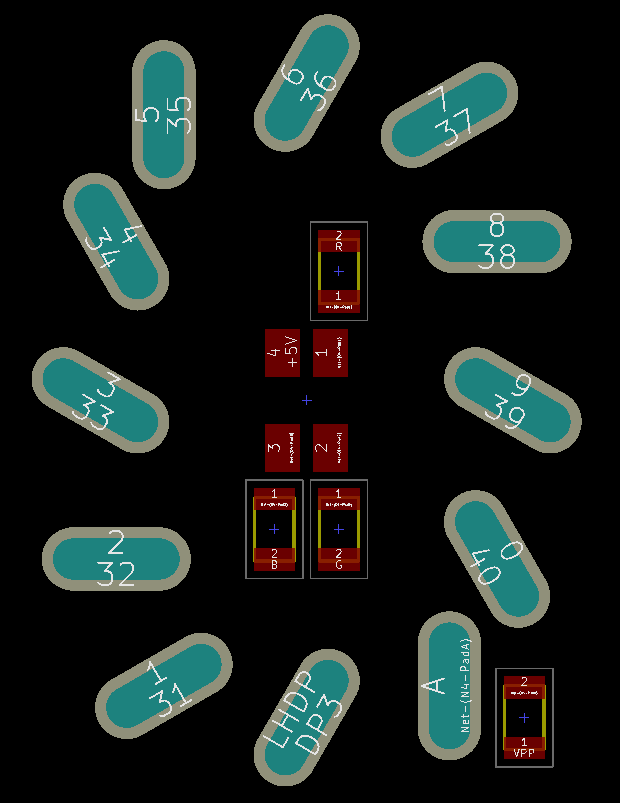
Segment 2

Segment 3

Segment 4

Segment 5

Figure - NTD Segment Arrangement



Digit 0

Digit 1

Digit 2

Digit 3

Digit 4

Digit 5

Digit 6

Digit 7

Digit 8

Digit 9

HV Input

DP

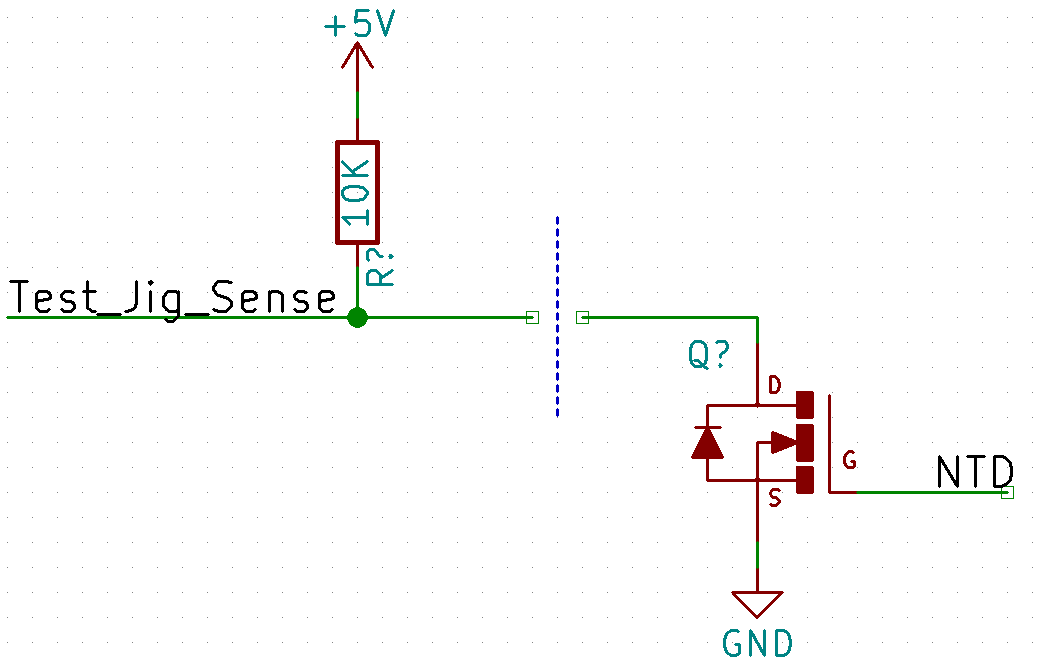
Figure - NTD Digit Arrangement

Combining this knowledge, the control bit stream is made up of 6 groups of 10 bit, corresponding to 1->9 followed by 0, followed by a group of 5 bits representing the decimal point.

On receipt of a ‘1’, the open drain MOSFET will be turned ‘ON’ and the net will be pulled to GND. On receipt of a ‘0’ the net will be High-Z, and will float.

**Theory of Test Operation**

The test for each net is simple. Each net will be pulled to +5V with a 10K resistor, it will then be commanded to turn ‘ON’ and enable its open drain FET. This should pull the voltage to 0V and a micro-controller can sense this. While the net is low the micro-controller will test every other net to make sure there are no other net’s also turning ‘ON’. This theory is illustrated below.

The high voltage lines will be tested by applying +5V at the socket, and testing whether we receive this at the header.

The main limit to this test method is it requires a micro-controller pin on every individual net, of which there are 66. This is undesirable, and would be difficult to route on the board. Thus it was decided to multiplex the test.

The groups for the multiplexing are split along segment, and along digit. This means that each segment will be able to be powered individually, and each digit group (all the 0s or all 1s etc.) can be tested at once. The digit’s not under test must be put in a Hi-Z state for this test to be effective.

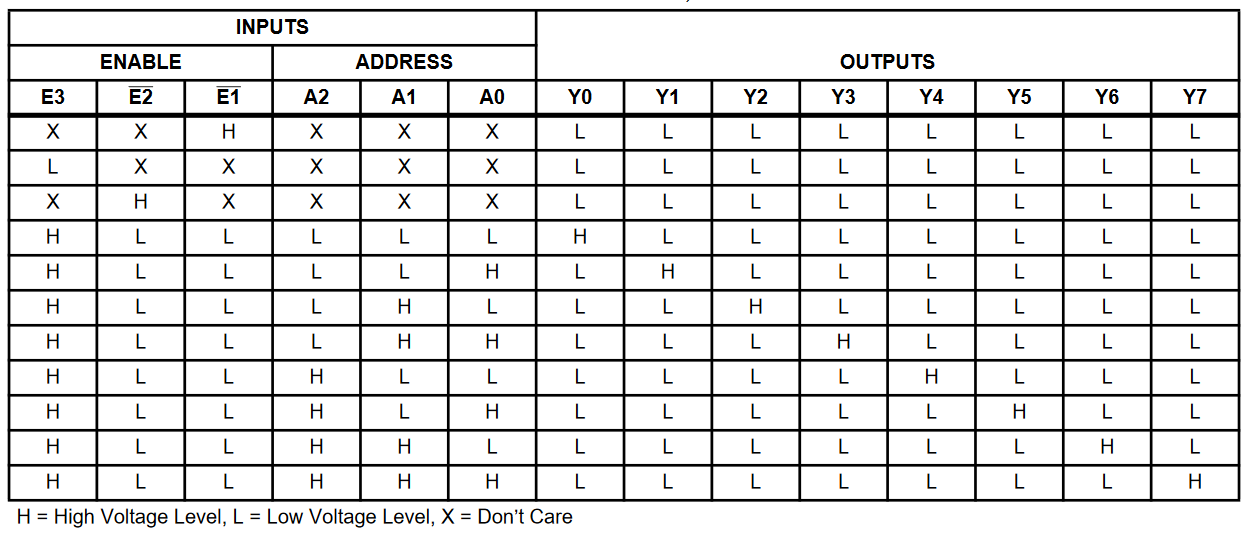
**Implementation**

*Micro-controller*

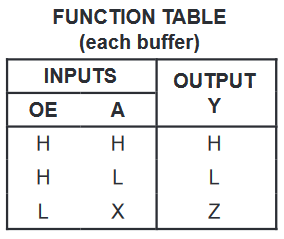
The micro-controller (uC) on the NTDTJ will be an ATMega328P-AU 32 pin TQFP uC. This will have the Arduino bootloader installed for ease of programming, and use of the pre-built NixieDriver library.

*Segment Decoding*

To facilitate the segment selection on the NTD test jig, a combination of a 3-8 line decoder and 2 tri-state buffer chips is used. The 3-8 line decoder is used to select which segment is active, and the tri-state buffers are used to put the segments not under test into the Hi-Z state required.



The truth table for the 74HC238 3-8 line decoder is given above. The address pins are connected to 3 of the ATMega output pins, and the E3 pin is also connected to the ATMega to use as an output enable pin. The #E2 and #E3 pins are tied low. Each output of the 74HC238 is tied to a 74HC126 tri-state buffer.

 The 74HC126 tri-state buffer has the ‘A’ and ‘OE’ input pins tied together, meaning the available states can be either High or Hi-Z.

The low state is not needed.

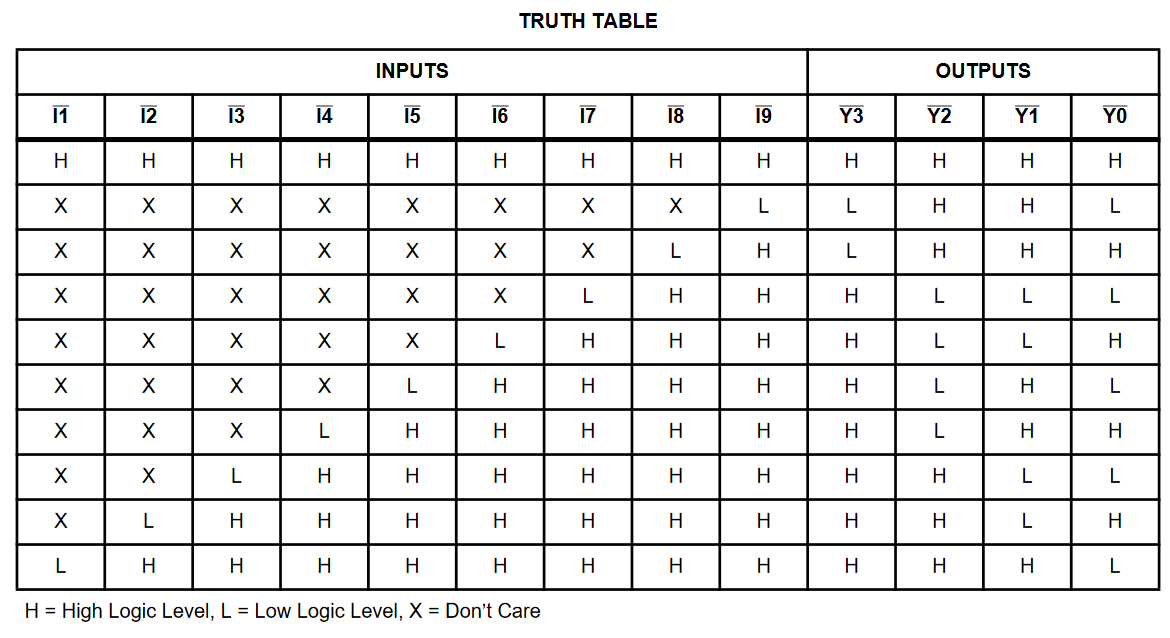
The following table is the combination of the function tables for the 74HC238 and the 74HC126:

(L = LOW, H = HIGH, X = Don’t Care, Z = Hi-Z)

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Outputs** | | | | | | | |
| **E3** | **A2** | **A1** | **A0** | **Y0** | **Y1** | **Y2** | **Y3** | **Y4** | **Y5** | **Y6** | **Y7** |
| L | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z |
| H | L | L | L | H | Z | Z | Z | Z | Z | Z | Z |
| H | L | L | H | Z | H | Z | Z | Z | Z | Z | Z |
| H | L | H | L | Z | Z | H | Z | Z | Z | Z | Z |
| H | L | H | H | Z | Z | Z | H | Z | Z | Z | Z |
| H | H | L | L | Z | Z | Z | Z | H | Z | Z | Z |
| H | H | L | H | Z | Z | Z | Z | Z | H | Z | Z |
| H | H | H | L | Z | Z | Z | Z | Z | Z | H | Z |
| H | H | H | H | Z | Z | Z | Z | Z | Z | Z | H |

*Digit Encoding*

The digits 1->9 from the NTD segments are encoded before being read into the ATMega with a 74HC147 priority encoder. The truth table is given below.

The digits are connected to their corresponding #I[N] pin. They will be read in order of 1 to 9, under the assumption that any short between the pins will be bi-directional (i.e. if #I2 goes low with #I7 it is assumed that #I7 will go low with #I2).

Digits 0 and DP are tied directly to the ATmega.

*Test Sequence*

The flowchart level description of the test sequence is given on the following page. The program will auto detect the presence of a NTD (by setting a segment HIGH and waiting for the HV input to go HIGH) and then proceed with the test.

The sketch will fade the RGBs in the background, whilst performing the functional test, the RGB fade will be timed to finish alongside the functional test.

Any errors encountered will be added to an error queue, which will be parsed out of the UART upon completion of the functional test. The RGBs will be used to give quick feedback on the outcome of the test.

